# Unit Vector Based HCC Strategy for a Buck–Boost Voltage/Current Source Inverter

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## Abstract

In recent years, research in hybrid electric vehicle (HEV) development has been focused on various aspect of design, such as component architecture, engine efficiency, reduced fuel emissions, material for lighter components, power electronics, efficient motors and high power density batteries. A DC–DC converter with a high step-up voltage gain is used for many applications, such as high-intensity discharge lamp ballasts for battery backup systems for continuation of power to the drive by utilizing the VSI or CSI topologies. This paper proposes a unit vector template based modulation (UVT) scheme with hysteresis current control strategy is preferred for a buck–boost voltage/ current source inverter. For a voltage source inverter, the switching loss is reduced by 92%, compared to a conventional space vector modulation scheme and optimization of THD is solely decreases, achieve quality nature of voltage to control the drive for EV applications. The dynamic analysis of proposed concept is implemented by using Matlab/Simulink Software Package and simulations results are presented, achieve high efficiency, high power density, high temperature, and low cost.

## 1 Introduction

Hybrid Electric Vehicle (HEV) is an emerging technology in the modern world because of the fact that it mitigates environmental pollutions and at the same time increases fuel efficiency of the vehicles. Voltage source inverter controls electric drive of HEV of high power and enhances its performance which is the reflection of the fact that it can generate sinusoidal voltages with only fundamental switching frequency and have almost no electromagnetic interference. This paper describes precisely various modulation techniques of HEVs and presents transformer less converter for high voltage and high current HEV in [1]. The inverter is IGBT based and it is fired in a sequence. It is natural fit for HEV as it uses separate level of dc sources which are in form of batteries or fuel cells. Compared to conventional vehicles, hybrid electric vehicles (HEVs) are more fuel efficient due to the optimization of the engine operation and recovery of kinetic energy during braking. With the plug-in option (PHEV), the vehicle can be operated on electric-only modes for a driving range of up
to 30–60 km. The PHEVs are charged overnight from the electric power grid where energy can be generated from renewable sources such as wind and solar energy.

Currently, two existing inverter topologies are used for hybrid electric vehicles (HEVs) and electric vehicles (EVs): the conventional three-phase inverter with a high voltage battery and a three-phase pulsewidth modulation (PWM) inverter with a dc/dc boost front end. The conventional PWM inverter imposes high stress on switching devices and motor thus limits the motor’s constant power speed range (CPSR), which can be alleviated through the dc–dc boosted PWM inverter. Fig. 1 shows a typical configuration of the series plug-in electric vehicle (PHEV) [2]. The inverter is required to inject low harmonic current to the motor, in order to reduce the winding loss and core loss. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the switching loss increase in switching device and also the core loss increase in the motor stator. To solve this problem, various soft-switching methods have. Active switching rectifier or a diode rectifier with small DC link capacitor is interfaced to this proposed EV applications through voltage source/current source inverter [3]-[5].

Varies types of modulation method have been proposed previously such as optimized pulsewidth-modulation improved, Space-Vector-PWM control for different optimization targets and applications and discontinuous PWM (DPWM). Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if an equal output THD is required, DPWM cannot reduce switching loss than SPWM. Moreover, it will worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been used to reduce the period of PWM switching to only 1/3 of the whole fundamental period. However, these papers didn’t compare the spectrum of this method with others, which is not fair. In addition, the method is only specified to a fixed topology, which cannot be applied widely [6],[7].

This paper proposes a novel generalized space vector pulsewidth amplitude modulation (SVPWAM) method for the buck/boost voltage source inverter (VSI) and current source inverter (CSI). By eliminating the conventional zero vectors in the space vector modulation, two-third and one-third switching frequency reduction can be achieved in VSI and CSI, respectively. If a unity power factor is assumed, an 87% switching loss reduction can be implemented in VSI, and a 74% reduction can be
implemented in CSI [8]-[12]. A 1-kW boost-converter inverter system has been developed and tested based on the SVPWAM method. Here authors prefer unit vector control strategy instead of SVPWM scheme because it is more complex compare to all other modulation schemes due to more number of vectors, so hard to design for more number of levels and prefer hysteresis based current control strategy have better features because controlled by unit vector control strategy, by using this technique get good THD response at output of the converter, may to reduce the load side filter value.

Space-vector pulse-with-modulation (SVPWM) is another technique of driving a voltage source three-phase H-bridge inverter, for generating voltage waveforms that are devoid of low-frequency harmonic content. The principle of an SVPWM control is to eliminate the zero vectors in each sector. The modulation principle of SVPWAM is shown in Fig.2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all. The dc-link voltage thus is directly generated from the output line-to-line voltage [13].

In sector I, no zero vectors are selected. Therefore, S1 and S2 keep constant ON, and S3 and S6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage $V_{ac}$ at this time [14]. Consequently, the dc-link voltage should present a $6\omega$ varied feature to maintain a desired output voltage. The topologies to implement this method will be discussed later. The original equations for time period $T_1$ and $T_2$ are

$$T_1 = \frac{\sqrt{3}}{2} m \sin \left( \frac{\pi}{3} - \theta \right); \quad T_2 = \frac{\sqrt{3}}{2} m \sin(\theta)$$  

2 Switching Loss Reduction For VSI Topology

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within $[-60^\circ, 60^\circ]$, at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage $V_{DC}$, and the current stress is equal to output current $i_a$. Thus the switching loss for each switch is

![Figure 2: SVPWAM for VSI.](image-url)
Where $E_{SR}$, $V_{ref}$, $I_{ref}$ are the references.

\[
P_{SW\perp} = \frac{1}{2\pi} \left[ \int_{-\pi/6}^{\pi/6} E_{SR} \left| I_m \sin(\omega t) \right| \cdot \frac{V_{DC}}{V_{ref}I_{ref}} \cdot f_{sw} \, d\omega t \right. \\
\left. + \int_{5\pi/6}^{7\pi/6} E_{SR} \left| I_m \sin(\omega t) \right| \cdot \frac{V_{DC}}{V_{ref}I_{ref}} \cdot f_{sw} \, d\omega t \right] \\
= \frac{2 - \sqrt{3}}{\pi} \cdot \frac{I_m V_{DC}}{V_{ref}I_{ref}} E_{SR} \cdot f_{sw}, \tag{2}
\]

Figure 3: Conventional CSI and its corresponding SVPWAM diagram.

Since the SVPWAM only has PWM switching in two 60° sections, the integration over $2\pi$ can be narrowed down into integration within two 60°

\[
P_{SW\perp} = \frac{2\sqrt{3}}{\pi} \cdot \left( I_m V_{DC} / \left( V_{ref}I_{ref} \right) \right) \cdot E_{SR} \cdot f_{sw}. \tag{4}
\]

The switching loss for a conventional SPWM method is

\[
P_{SW\perp'} = \frac{2}{\pi} \cdot \left( I_m V_{DC} / \left( V_{ref}I_{ref} \right) \right) \cdot E_{SR} \cdot f_{sw}. \tag{5}
\]

In result, the switching loss of SVPWAM over SPWM is $f = 13.4\%$. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases. As indicated, the worst case happens when power factor is equal to zero, where the
switching loss reduction still reaches 50% in [15]. In conclusion, SVPWAM can bring the switching loss down by 50–87%.

3 Unit Vector Control Strategy

![Diagram: Block diagram representation of grid-interfacing inverter control.](image)

The control diagram for a three phase inverter is shown in Fig. 4. The regulation of dc-link voltage carries the information regarding the exchange of active power in between inverter. Thus the output of dc-link voltage regulator results in an active current (Im). The multiplication of active current component (Im). With unity grid voltage vector templates (U_a, U_b, and U_c) generates the reference voltages and currents (I_a*, I_b*, and I_c*). The grid synchronizing angle (θ) obtained from phase locked loop (PLL) is used to generate unity vector template as [9]–[16]

\[
U_a = \sin(\theta) \\
U_b = \sin(\theta - \frac{2\pi}{3}) \\
U_c = \sin(\theta + \frac{2\pi}{3})
\]

(6) (7) (8)

The actual dc-link voltage (V_{dc}) is sensed and passed through a first-order low pass filter (LPF) to eliminate the presence of switching ripples on the dc-link voltage and in the generated reference current signals [17]–[19]. The difference of this filtered dc-link voltage and reference dc-link voltage \(V_{dc}^*(n)\) is given to a discrete-PI regulator to maintain a constant dc-link voltage under varying generation and load conditions. The dc-link voltage error \(V_{dcerr}(n) = V_{dc}^*(n) - V_{dc}(n)\).

\[
I_{m}(n) = I_{m}(n-1) + K_{F_{dc}}(V_{dcerr}(n) - V_{dcerr}(n-1)) \\
+ K_{I_{dc}}V_{dcerr}(n)
\]

(9)

Where \(K_{F_{dc}} = 10\) and \(K_{I_{dc}} = 0.05\) are proportional and integral gains of dc-voltage regulator.

The output of discrete-PI regulator at nth sampling instant is expressed as

\[
I_{m}(n) = I_{m}(n-1) + K_{F_{dc}}(V_{dcerr}(n) - V_{dcerr}(n-1)) \\
+ K_{I_{dc}}V_{dcerr}(n)
\]

(10)

The instantaneous values of reference three phase grid currents are computed as

\[
I_a^* = I_m \cdot U_a \\
I_b^* = I_m \cdot U_b \\
I_c^* = I_m \cdot U_c
\]

(11) (12) (13)
The reference currents ($I_a^*$, $I_b^*$, $I_c^*$ and $I_n^*$) are compared with actual grid currents ($I_a$, $I_b$, $I_c$ and $I_n$) to compute the current errors as

\[
I_{aerr} = I_a^* - I_a
\]  
(14)

\[
I_{berr} = I_b^* - I_b
\]  
(15)

\[
I_{cerr} = I_c^* - I_c
\]  
(16)

\[
I_{nerr} = I_n^* - I_n
\]  
(17)

These current errors are given to hysteresis current controller. The hysteresis controller then generates the switching pulses ($P_1$ to $P_8$) for the gate drives of interfacing inverter. The average model of 4-leg inverter can be obtained by the following state space equations

\[
\frac{dI_{Inv_a}}{dt} = \frac{(V_{Inv_a} - V_a)}{L_{sh}}
\]  
(18)

\[
\frac{dI_{Inv_b}}{dt} = \frac{(V_{Inv_b} - V_b)}{L_{sh}}
\]  
(19)

\[
\frac{dI_{Inv_c}}{dt} = \frac{(V_{Inv_c} - V_c)}{L_{sh}}
\]  
(20)

\[
\frac{dI_{Inv_n}}{dt} = \frac{(V_{Inv_n} - V_n)}{L_{sh}}
\]  
(21)

\[
\frac{dV_{dc}}{dt} = \frac{(I_{Inv_a} + I_{Inv_b} + I_{Inv_c} + I_{Inv_n})}{C_{dc}}
\]  
(22)

Where $V_{Inv_a}$, $V_{Inv_b}$, $V_{Inv_c}$ and $V_{Inv_n}$ are the three-phase ac switching voltages generated on the output terminal of inverter. These inverter output voltages can be modeled in terms of instantaneous dc bus voltage and switching pulses of the inverter as

\[
V_{Inv_a} = \frac{(P_1 - P_2)}{2} V_{dc}
\]  
(23)

\[
V_{Inv_b} = \frac{(P_3 - P_6)}{2} V_{dc}
\]  
(24)

\[
V_{Inv_c} = \frac{(P_4 - P_5)}{2} V_{dc}
\]  
(25)

\[
V_{Inv_n} = \frac{(P_7 - P_8)}{2} V_{dc}
\]  
(26)

Similarly the charging currents $V_{Inv_a}$, $V_{Inv_b}$, $V_{Inv_c}$ and $V_{Inv_n}$ on dc bus due to the each leg of inverter can be expressed as

\[
I_{Inv_a} = I_{Inv_a}(P_1 - P_4)
\]  
(27)

\[
I_{Inv_b} = I_{Inv_b}(P_3 - P_6)
\]  
(28)

\[
I_{Inv_c} = I_{Inv_c}(P_5 - P_2)
\]  
(29)

\[
I_{Inv_n} = I_{Inv_n}(P_7 - P_8)
\]  
(30)

The switching pattern of each IGBT inside inverter can be formulated on the basis of error between actual and reference current of inverter, which can be explained as: If $I_{Inv_a} < (I_{Inv_a} - h_b)$, then upper switch $S_1$ will be OFF ($P_1 = 0$) and lower switch $S_4$ will be ON ($P_4 = 1$) in the phase “a” leg of inverter. If $I_{Inv_a} > (I_{Inv_a} - h_b)$, then upper switch $S_1$ will be ON ($P_1 = 1$) and lower switch $S_4$ will be OFF ($P_4 = 0$) in the phase “a” leg of inverter. Where $h_b$ is the width of hysteresis band. On the same principle, the switching pulses for the other remaining three legs can be derived [20].
4 Matlab/Simulink Modeling And Results

Here simulation is carried out in several cases, in that here simulation is carried out in several configurations, in that

- Proposed Current Source Inverter Operating Under Space Vector Modulation Scheme
- Proposed Current Source Inverter Operating Under Unit Vector Modulation Scheme

Case A: Proposed Current Source Inverter Operating Under Space Vector Modulation Scheme

![Matlab/Simulink Model of Proposed Vector Controlled Modulation Scheme for 2-level CSI Topology](image)

Fig. 5 Matlab/Simulink Model of Proposed Vector Controlled Modulation Scheme for 2-level CSI Topology

Fig. 5 shows the Matlab/Simulink Model of Proposed Vector Controlled Modulation Scheme for 2-level CSI Topology using MATLAB/SIMULINK platform, the inverter is controlled by using proposed space vector modulation scheme, it is more effective compared to conventional modulation schemes and preferred in many industrial applications.
Fig. 6 (a) PV Output Voltage, (b) Switching States of Proposed Vector Controlled Modulation Scheme for 2-level CSI Topology for Drive Applications.

Fig. 7 Output Voltage, Output Current, DC Link Current, of Proposed Vector Controlled Modulation Scheme before filter for 3-level CSI Topology for Drive Applications.

(a) Output Voltage & Current

(b) Output Voltage THD

Fig. 8 Output Voltage & Current, THD of Proposed Vector Controlled Modulation Scheme with filter for 3-level CSI Topology for Drive Applications.
Case 02: Proposed Current Source Inverter Operating Under Unit Vector Modulation Scheme

Fig. 9 Output Voltage, Output Current, DC Link Current, of Proposed Unit Vector Controlled Scheme before filter for 3-level CSI Topology for Drive Applications

Fig. 10 Output Voltage, THD of Proposed Unit Vector Controlled Scheme for 3-level CSI Topology for Drive Applications
5 Conclusion

Here proposed to compare the operation of unit vector controller strategy with HCC technique and SVPWM control method have better features with preserves the following advantages compared to traditional SPWM and SVPWM method. The switching power loss is reduced by 90% compared with the conventional SPWM inverter system. The power density is increased by a factor of 2 because of reduced dc capacitor (from 40 to 6 μF) and small heat sink is needed. The cost is reduced by 30% because of reduced passives, heat sink, and semiconductor stress. The effectiveness of the proposed method in reduction of power losses has been validated by the simulation results that were obtained from the Matlab/simulation model.

6 References


**BIOGRAPHIES**

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